**CLAIMS**:

1. A radio frequency identification device comprising:

a monolithic integrated circuit including a receiver, a transmitter, and a microprocessor.

2. A radio frequency identification device in accordance with claim 1 wherein the receiver and transmitter together define an active transponder, and wherein the device comprises a battery supplying power to the integrated circuit.

3. A radio frequency identification device comprising:

a monolithic integrated circuit including a receiver, a transmitter which can operate at frequencies above 400 MHz, and a microprocessor.

4. A radio frequency identification device comprising:

a monolithic integrated circuit including a receiver, a transmitter which can operate at frequencies above 1 GHz, and a microprocessor.

5. A radio frequency identification device comprising:

a monolithic integrated circuit including a transmitter, a microprocessor, and a receiver which can receive and interpret signals having frequencies above 400 MHz.

6. A radio frequency identification device comprising:

a monolithic integrated circuit including a transmitter, a microprocessor, and a receiver which can receive and interpret signals having frequencies above 1 GHz.

7. A radio frequency identification device comprising:

a monolithic integrated circuit including a receiver, a microwave transmitter, and a microprocessor.

8. A radio frequency identification device in accordance with claim 7 wherein the receiver and transmitter together define an active transponder.

9. A radio frequency identification device in accordance with claim 7 wherein the receiver is a microwave receiver.

10. A radio frequency identification device comprising:

a monolithic integrated circuit including a microwave receiver, a transmitter, and a microprocessor.

11. A radio frequency identification device in accordance with claim 10 wherein the receiver and transmitter together define an active transponder.

12. A radio frequency identification device in accordance with claim 10 wherein the transmitter is a microwave transmitter.

13. A radio frequency identification device comprising:

a single die including a receiver, a transmitter, and a microprocessor, the die having a size less than 90,000 $mils^2$.

14. A radio frequency identification device in accordance with claim 13 wherein the die has a size less than 300 x 300 $mils^2$.

15. A radio frequency identification device in accordance with claim 13 wherein the die has a size less than 37,500 $mils^2$.

16. A radio frequency identification device in accordance with claim 13 wherein the die has a size less than 250 x 150 $mils^2$.

17. A radio frequency identification device comprising:

a single die including a receiver, a transmitter, and a microprocessor, the die having a size of substantially 209 by substantially 116 $mils^2$.

18. A radio frequency identification device comprising:

a single die integrated circuit including a receiver, a transmitter, and a microprocessor.

19. A radio frequency identification device in accordance with claim 18 wherein the receiver and transmitter together define an active transponder, and wherein the device comprises a battery supplying power to the integrated circuit.

20. A radio frequency identification device comprising:

a single die with a single metal layer including a receiver, a transmitter, and a microprocessor.

21. A radio frequency identification device in accordance with claim 20 wherein the receiver and transmitter together define an active transponder, and wherein the device comprises a battery supplying power to the integrated circuit.

22. A radio frequency identification device comprising:

a single die integrated circuit including a receiver, a transmitter, and a microprocessor formed using a single metal layer processing method.

23. A radio frequency identification device in accordance with claim 22 wherein the receiver and transmitter together define an active transponder, and wherein the device comprises a battery supplying power to the integrated circuit.

24. A radio frequency identification system comprising:

an integrated circuit including a receiver, and a transmitter; and

an antenna coupled to the integrated circuit, the integrated circuit being responsive to radio frequency signals of multiple carrier frequencies.

25. A radio frequency identification system in accordance with claim 24 wherein the receiver comprises a Schottky diode detector.

26. A radio frequency identification system in accordance with claim 24 wherein the transmitter comprises a modulated backscatter transmitter.

27. A radio frequency identification system in accordance with claim 24 wherein the integrated circuit receives commands from an interrogator transmitting a radio frequency signal including a series of digital data bits modulated on a carrier, the carrier having a carrier frequency, wherein the integrated circuit uses the frequency of data bits modulated on the carrier but does not use the carrier frequency.

28. A radio frequency identification device comprising:

transponder circuitry formed in a monolithic integrated circuit comprising both transmitting and receiving circuits of the transponder circuitry;

a power supply operably associated with the transponder circuitry; and

an antenna operably associated with the transponder circuitry.

29. A radio frequency identification device comprising:

a monolithic semiconductor integrated circuit including a receiver and a transmitter;

means for applying a supply of power to the integrated circuit device from a battery; and

means for configuring the integrated circuit to receive and transmit radio frequency signals.

30. A method for producing a radio frequency identification device (RFID), the method comprising the following steps:

providing a monolithic integrated circuit having a receiver and a transmitter; and

providing a package configured to carry the integrated circuit.

31. A method in accordance with claim 30, the configuring step including providing an antenna coupled with the integrated circuit and configurable to enable at least one of signal transmitting and signal receiving.

32. A method for adapting a radio frequency data communication device for use at a desired carrier frequency for use in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having tunable circuitry, the integrated circuit comprising a receiver and a transmitter;

configuring the integrated circuit for connection with a power supply to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; and

tuning the tunable circuitry and the antenna to realize a desired carrier frequency from a wide range of possible carrier frequencies.

33. A method for adapting a radio frequency data communication device for use at a desired carrier frequency for use in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having tunable circuitry, the integrated circuit comprising a receiver and a transmitter;

configuring the integrated circuit for connection with a power supply to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; and

tuning the antenna to realize a desired carrier frequency from a wide range of possible carrier frequencies.

34. A radio frequency communications device comprising:

an integrated circuit including a transmitter and a receiver, the integrated circuit including a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop including a voltage controlled oscillator, and a loop filter having a capacitor storing a voltage indicative of a frequency at which the voltage controlled oscillator is oscillating, the integrated circuit using the voltage stored on the capacitor to generate a clock frequency for the transmitter.

35. A radio frequency communications device in accordance with claim 34 and further comprising circuitry using the voltage stored on the capacitor to produce a clock signal for generating a transmitter carrier frequency.

36. A radio frequency communications device in accordance with claim 34 wherein the transmitter transmits using differential phase shift keying, and further comprising circuitry using the voltage stored on the capacitor to produce a clock signal, and divider circuitry dividing the clock frequency to generate tones for differential phase shift keyed transmission.

37. A method of recovering a clock frequency from a received radio frequency signal, storing the clock frequency, and using the clock frequency for radio frequency transmission by a transmitter, the method comprising:

providing a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop including a voltage controlled oscillator, and a loop filter having a capacitor;

using the clock recovery circuit to recover a clock frequency from a received radio frequency signal;

storing on the capacitor a voltage indicative of frequency at which the voltage controlled oscillator is oscillating;

using the voltage stored on the capacitor to generate a clock frequency for use by the transmitter.

38. A method in accordance with claim 37 and further comprising the step using the voltage stored on the capacitor to produce a clock signal for generating a transmitter carrier frequency.

39. A method in accordance with claim 37 and further comprising the step of using the voltage stored on the capacitor to produce a clock signal for generating tones for frequency shift keyed transmission.

40. A method in accordance with claim 37 and further comprising the step of dividing the recovered clock frequency for generating tones for differential phase shift keyed transmission.

41. A method of recovering and storing a clock frequency from a received radio frequency signal in a radio frequency identification device including a transmitter and a receiver, the method comprising:

providing a clock recovery circuit recovering a clock frequency from a signal received by the receiver, the clock recovery circuit having a phase lock loop;

using the clock recovery circuit to recover a clock frequency from a received radio frequency signal;

storing in analog form a value indicative of frequency at which the voltage controlled oscillator is oscillating;

using the analog value to generate a clock frequency for use by the transmitter.

42. A radio frequency communications device comprising:

an integrated circuit including a transmitter and a receiver, the transmitter being switchable between a backscatter mode, wherein a carrier for the transmitter is derived from a carrier received from an interrogator spaced apart from the radio frequency communications device, and an active mode, wherein a carrier for the transmitter is generated by the integrated circuit itself.

43. A radio frequency communications device in accordance with claim 42 wherein the transmitter switches between the backscatter and active modes in response to a radio frequency command received by the receiver.

44. A radio frequency communications device comprising:

an integrated circuit including a transmitter and a receiver, the transmitter selectively transmitting a signal using a modulation scheme, the transmitter being switchable for transmission using different modulation schemes.

45. A radio frequency communications device in accordance with claim 44 wherein the transmitter is switchable between at least two modulation schemes selected from the group consisting of Frequency Shift Keying (FSK), Binary Phase Shift Keying (BPSK), Direct Sequence Spread Spectrum, On-Off Keying (OOK), Amplitude Modulation (AM), and Modulated Backscatter (MBS).

46. A method for adapting modulation schemes of a radio frequency data communication device in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having switching circuitry, a receiver, a transmitter, and a processor; the integrated circuit having a plurality of transmitting circuits including a first transmitting circuit configured to realize an active transmitter scheme and a second transmitting circuit configured to realize a modulated backscatter scheme;

configuring the integrated circuit for connection with a power supply to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation; and

switching the switchable circuitry with respect to the antenna to enable one of the transmitting circuits to realize one of the modulation schemes.

47. A method for adapting modulation schemes of a radio frequency data communication device in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having switching circuitry, a receiver, a transmitter, and a processor, the integrated circuit including a plurality of transmitting circuits, the plurality of transmitting circuits configured to selectively realize a plurality of modulated backscatter schemes;

configuring the integrated circuit for connection with a power supply to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation; and

switching the transmitting circuits with respect to the antenna to enable one of the transmitting circuits to realize one of the modulation schemes.

48. A radio frequency identification device comprising:

an integrated circuit including a transmitter and a receiver, the integrated circuit being adapted to be connected to a battery, and further including a comparator comparing the voltage of the battery with a predetermined voltage and generating a low battery signal if the voltage of the battery is less than the predetermined voltage.

49. A radio frequency identification device in accordance with claim 48 wherein the integrated circuit further comprises a band gap voltage generator which generates a reference voltage, and wherein the predetermined voltage is the reference voltage produced by the band gap voltage generator.

50. A radio frequency identification device in accordance with claim 48 wherein the integrated circuit responds to commands received by the receiver from an interrogator, wherein the integrated circuit comprises a status register having a value indicating whether battery voltage is less than the predetermined voltage and wherein the transmitter transmits the value of the status register in response to a command received by the receiver.

51. A radio frequency identification device in accordance with claim 48 wherein the transmitter selectively transmits the low battery signal using a radio frequency signal.

52. A method for detecting a low battery condition in a radio frequency data communication device for use in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having switching circuitry, a receiver, and a transmitter, the integrated circuit including a comparator configured to compare the battery voltage with a predetermined voltage and generate a low battery signal if the battery voltage is less than the predetermined voltage;

configuring the integrated circuit for connection with the battery to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between;

determining a predetermined voltage for the battery;

comparing the voltage of the battery with the predetermined voltage; and

generating a low battery signal if the voltage of the battery is less than the predetermined voltage.

53. A radio frequency communications device comprising:

an integrated circuit including a transmitter and a receiver, the integrated circuit periodically checking if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a frequency lock loop.

54. A radio frequency communications device in accordance with claim 53 wherein the frequency lock loop comprises a current controlled oscillator.

55. A radio frequency communications device in accordance with claim 53 wherein the integrated circuit is configured to recover a clock frequency from the received signal and wherein the transmitter is configured to use the recovered clock frequency.

56. A radio frequency communications device in accordance with claim 53 wherein the integrated circuit switches between a sleep mode, and a higher power mode in which more power is consumed than in the sleep mode.

57. A radio frequency communications device in accordance with claim 53 and further comprising a variable value divider connected to the output of the frequency lock loop, the value of the divider being programmable in response to a radio frequency signal received by the receiver so as to program the time period of the checking.

58. A radio frequency communications device in accordance with claim 53 wherein the device is configured to receive and process commands from an interrogator transmitting a radio frequency signal and to enable the frequency lock loop only during processing of a command, to calibrate the timer to a clock frequency recovered from a received command.

59. A radio frequency communications device comprising:

an integrated circuit including a transmitter and a receiver, the integrated circuit being configured to periodically check if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a phase lock loop.

60. A radio frequency communications device in accordance with claim 59 wherein a clock frequency is recovered from the received signal and used by the transmitter.

61. A radio frequency communications device in accordance with claim 59 wherein the phase lock loop comprises a current controlled oscillator.

62. A radio frequency communications device in accordance with claim 59 wherein the integrated circuit switches between a sleep mode, and a higher power mode in which more power is consumed than in the sleep mode.

63. A radio frequency communications device in accordance with claim 59 and further comprising a variable value divider connected to the output of the phase lock loop, the value of the divider being programmable in response to a radio frequency signal received by the receiver so as to program the time period for the checking.

64. A radio frequency communications device in accordance with claim 59 wherein the device receives and processes commands from an interrogator transmitting a radio frequency signal, and wherein the phase lock loop is enabled only during processing of a command, to calibrate the timer to a clock frequency recovered from a received command.

65. A method for calibrating a clock in a radio frequency data communication device for use in a radio frequency identification (RFID) device, the method comprising the following steps:

providing an integrated circuit having a receiver and a transmitter, the integrated circuit including a timer having a frequency lock loop configured to set a time period for periodically checking if a radio frequency signal is being received by the receiver;

configuring the integrated circuit for connection with a battery to enable operation;

configuring the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation therebetween; and

periodically checking whether a radio frequency signal is being received by the receiver.

66. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received via the connection pin.

67. A radio frequency identification device in accordance with claim 66 wherein the connection pin is a serial input pin.

68. A radio frequency identification device in accordance with claim 66 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency receive mode and the direct receive mode in response to a signal applied to the selection pin.

69. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a digital input pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received digitally via the digital input pin.

70. A radio frequency identification device in accordance with claim 69 wherein the digital input pin is a serial input pin.

71. A radio frequency identification device in accordance with claim 69 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency receive mode and the direct receive mode in response to a signal applied to the selection pin.

72. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein a modulation signal without a carrier is received via the connection pin.

73. A radio frequency identification device in accordance with claim 72 wherein the connection pin is a serial input pin.

74. A radio frequency identification device in accordance with claim 72 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency receive mode and the direct receive mode in response to a signal applied to the selection pin.

75. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted via the connection pin.

76. A radio frequency identification device in accordance with claim 75 wherein the connection pin is a serial output pin.

77. A radio frequency identification device in accordance with claim 75 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency transmit mode and the direct transmit mode in response to a signal applied to the selection pin.

78. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a digital output pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted digitally via the digital output pin.

79. A radio frequency identification device in accordance with claim 78 wherein the connection pin is a serial output pin.

80. A radio frequency identification device in accordance with claim 78 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency transmit mode and the direct transmit mode in response to a signal applied to the selection pin.

81. A radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising:

an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein a modulation signal without a carrier is transmitted via the connection pin.

82. A radio frequency identification device in accordance with claim 81 wherein the connection pin is a serial output pin.

83. A radio frequency identification device in accordance with claim 81 and further comprising a selection pin, and wherein the integrated circuit switches between the radio frequency transmit mode and the direct transmit mode in response to a signal applied to the selection pin.

84. A method comprising the following steps:

providing an integrated circuit having a receiver, a transmitter, and a connection pin, the integrated circuit including a switchable circuit configured to switch between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received via the connection pin;

configuring the integrated circuit for connection with a battery;

configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and

switching to one of the radio frequency receive mode and the direct receive mode to enable receipt of radio frequency commands or commands received via the connection pin.

85. A method comprising the following steps:

providing an integrated circuit having a receiver, a transmitter, and a connection pin, the integrated circuit including a switchable circuit configured to switch between a radio frequency transmit mode wherein the transmitter transmits information via radio frequency, and a direct transmit mode wherein data is transmitted via the connection pin;

configuring the integrated circuit for connection with a battery;

configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and

switching to one of the radio frequency transmit mode and the direct transmit mode to enable transmission of information via radio frequency or via the connection pin.

86. An integrated circuit comprising:

a radio frequency receiver;

a unique, non-alterable indicia identifying the integrated circuit; and

a radio frequency transmitter configured to transmit a signal representative of the indicia in response to a command received by the receiver.

87. An integrated circuit in accordance with claim 86 and further comprising an antenna coupled to the integrated circuit, a battery coupled to the integrated circuit and powering the integrated circuit, and a tag housing encapsulating the integrated circuit, battery, and antenna.

88. An integrated circuit in accordance with claim 86 wherein the integrated circuit comprises a programmable read only memory, and wherein the non-alterable indicia is burned into the programmable read only memory.

89. An integrated circuit in accordance with claim 86 wherein the non-alterable indicia comprises laser blown polysilicon links.

90. An integrated circuit in accordance with claim 86 wherein the integrated circuit comprises an EEPROM containing the non-alterable indicia.

91. An integrated circuit in accordance with claim 86 wherein the integrated circuit comprises a flash ROM containing the non-alterable indicia.

92. A radio frequency identification device comprising:

an integrated circuit including a receiver for receiving radio frequency commands from an interrogation device, and a transmitter for transmitting a signal identifying the device to the interrogator, the transmitter and receiver being formed on a die having a lot number, wafer number, and die number, the integrated circuit including non-alterable indicia identifying the lot number, wafer number, and die number, the transmitter being configured to transmit the non-alterable indicia in response to a manufacturer's command received by the receiver, the transmitted non-alterable indicia being different from the identifying signal.

93. A radio frequency identification device in accordance with claim 92 wherein the integrated circuit comprises a programmable read only memory, and wherein the non-alterable indicia is burned into the programmable read only memory.

94. An integrated circuit in accordance with claim 92 wherein the non-alterable indicia comprises laser blown polysilicon links.

95. An integrated circuit in accordance with claim 92 wherein the integrated circuit comprises an EEPROM containing the non-alterable indicia.

96. An integrated circuit in accordance with claim 92 wherein the integrated circuit comprises a flash ROM containing the non-alterable indicia.

97. A radio frequency identification device in accordance with claim 92 and further comprising an antenna coupled to the integrated circuit, a battery coupled to the integrated circuit and powering the integrated circuit, and a tag housing encapsulating the integrated circuit, battery, and antenna.

98. A method of tracing manufacturing process problems by tracing the origin of a defective radio frequency identification integrated circuit, the method comprising:

forming a non-alterable indicia on a die for the integrated circuit, the indicia representing the wafer lot number, wafer number, and die number on the wafer, the indicia being not readily ascertainable by a user; and

causing the integrated circuit to transmit the non-alterable indicia via radio frequency in response to a manufacturer's command.

99. A method of tracing stolen property including a radio frequency identification integrated circuit, the method comprising:

forming a non-alterable indicia on a die for the integrated circuit, the indicia representing the wafer lot number, wafer number, and die number on the wafer, the indicia being not readily ascertainable by a user; and

causing the integrated circuit to transmit the non-alterable indicia via radio frequency in response to a manufacturer's command.

100. A method of tracing manufacturing process problems in the manufacture of a radio frequency integrated circuit by tracing defect origin, the method comprising the following steps:

providing a detectable signature on the integrated circuit, the signature indicative of one or more of the wafer lot number, wafer number, and die number of a die for the integrated circuit; and

enabling the integrated circuit to transmit the signature via radio frequency responsive to an inquiry command.

101. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a receiver receiving radio frequency commands from an interrogation device, and a transmitter transmitting a signal identifying the device to the interrogator, the integrated circuit switching between a sleep mode, and a microprocessor on mode, in which more power is consumed than in the sleep mode, if the microprocessor determines that a signal received by the receiver is a radio frequency command from an interrogation device.

102. A method for conserving power during operation of a radio frequency identification device (RFID), the method comprising the following steps:

providing a receiver, a transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry configured to selectively supply clock signals to the processor and thus control power consumption of the processor;

configuring the receiver with an antenna to receive radio frequency signals from an interrogation device,

configuring the transmitter to transmit a signal identifying the device to the interrogator;

selectively enabling powered wake-up of the receiver to periodically check for presence of radio frequency signals;

detecting whether a radio frequency signal is valid; and

depending on whether a radio frequency signal is valid, supplying clock signals to the processor.

103. A method in accordance with claim 102 wherein the receiver, the transmitter, and the wake-up circuitry are provided on an integrated circuit.

104. A method for conserving power during operation of a radio frequency identification device (RFID), the method comprising the following steps:

providing a receiver, a transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry configured to selectively supply power to the processor;

configuring the receiver with an antenna to receive radio frequency signals from an interrogation device,

configuring the transmitter to transmit a signal identifying the device to the interrogator;

selectively enabling powered wake-up of the receiver to periodically check for presence of radio frequency signals;

detecting whether a radio frequency signal is valid; and

depending on whether a radio frequency signal is valid, supplying power signals to the processor.

105. A method in accordance with claim 104 wherein the receiver, the transmitter, and the wake-up circuitry are provided on an integrated circuit.

106. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit being switchable between a sleep mode, and a microprocessor on mode in which more power is consumed than in the sleep mode, the integrated circuit being switched from the sleep mode to the microprocessor on mode in response to a direct sequence spread spectrum modulated radio frequency signal, which has a predetermined number of transitions within a certain period of time, being received by the receiver.

107. A method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present:

(a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; and

(b) determining if the radio frequency signal has a predetermined number of transitions per a predetermined time period and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

108. A method in accordance with claim 107 wherein the radio frequency identification device further comprises a clock recovery circuit recovering a clock from incoming radio frequency signals, the clock recovery circuit including a phase lock loop and wherein the tests further comprise determining whether frequency lock is achieved on the incoming radio frequency signal within a predetermined number of transitions.

109. A radio frequency identification device switchable between a sleep mode and a mode in which more power is consumed than in the sleep mode, the radio frequency identification device comprising:

a transponder including a receiver and a transmitter;

means for periodically checking whether any radio frequency signal is being received by the receiver; and

means for determining if a radio frequency signal has a predetermined number of transitions within a predetermined period of time.

110. A method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present:

(a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode;

(b) determining if the radio frequency signal is modulated and has a predetermined number of transitions per a predetermined period of time and, if so, proceeding to step (c); and, if not, returning to the sleep mode; and

(c) determining if the modulated radio frequency signal has a predetermined number of transitions per a predetermined period of time different from the predetermined time of step (b) and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

111. A method in accordance with claim 110 wherein the radio frequency identification device further comprises a clock recovery circuit recovering a clock from incoming radio frequency signals, the clock recovery circuit including a phase lock loop and wherein the tests further comprise determining whether frequency lock is achieved on the incoming radio frequency signal within a predetermined amount of time.

112. A method of forming an integrated circuit including a Schottky diode, the method comprising:

providing a p-type substrate;

defining an n-type region relative to the substrate;

forming an insulator over the n-type region;

removing an area of the insulator for definition of a contact hole, and removing an area encircling the contact hole;

forming n+regions in the n-type regions encircling the contact hole;

depositing a Schottky metal in the contact hole; and

annealing the metal to form a silicide interface to the n-type region.

113. A method in accordance with claim 112 and further comprising depositing tungsten into the contact hole.

114. A method in accordance with claim 113 wherein the tungsten is deposited by chemical vapor deposition.

115. A method in accordance with claim 113 and further comprising planarizing the tungsten.

116. A method of forming an integrated circuit including a Schottky diode, the method comprising:

providing a substrate;

defining a p-type region relative to the substrate;

forming an insulator over the p-type region;

removing an area of the insulator for definition of a contact hole, and removing an area encircling the contact hole;

forming p+regions in the p-type regions encircling the contact hole;

depositing a Schottky metal in the contact hole; and

annealing the Schottky metal to form a silicide interface to the p-type region.

117. A method in accordance with claim 116 and further comprising depositing tungsten into the contact hole.

118. A method in accordance with claim 117 wherein the tungsten is deposited by chemical vapor deposition.

119. A method in accordance with claim 117 and further comprising planarizing the tungsten

120. A method of forming an integrated circuit including a Schottky diode, the method comprising:

providing a p-type substrate;

defining an n-well region relative to the substrate;

forming a BPSG insulator over the n-well region;

etching away an area of the BPSG for definition of a contact hole, and etching an area encircling the contact hole;

forming n+regions in the n-well regions encircling the contact hole;

depositing titanium in the contact hole; and

annealing the titanium to form a silicide interface to the n-well region.

121. A method in accordance with claim 120 and further comprising depositing tungsten into the contact hole.

122. A method in accordance with claim 121 wherein the tungsten is deposited by chemical vapor deposition.

123. A method in accordance with claim 121 and further comprising planarizing the tungsten.

124. A method of forming an integrated circuit including a Schottky diode, the method comprising:

providing an n-type substrate;

defining a p-well region relative to the substrate;

forming a BPSG insulator over the p-well region;

etching away an area of the BPSG for definition of a contact hole, and etching an area encircling the contact hole;

forming p+regions in the p-well regions encircling the contact hole;

depositing titanium in the contact hole; and

annealing the titanium to form a silicide interface to the p-well region.

125. A method in accordance with claim 124 and further comprising depositing tungsten into the contact hole.

126. A method in accordance with claim 125 wherein the tungsten is deposited by chemical vapor deposition.

127. A method in accordance with claim 125 and further comprising planarizing the tungsten.

128. A radio frequency communications system comprising:

an antenna;

an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode coupled to the antenna; and

a current source connected to drive current through the antenna and the Schottky diode.

129. A radio frequency communications system in accordance with claim 128 wherein the receiver is inductorless.

130. An integrated circuit for radio frequency communications comprising an inductorless radio frequency detector.

131. A system comprising:

an antenna;

a transponder including a receiver having a Schottky diode detector including a Schottky diode having a first terminal coupled to the antenna and having a second terminal; and

means for driving current through both the antenna and the Schottky diode in a direction from the first terminal to the second terminal.

132. A system comprising:

an antenna;

a transponder including a receiver having a Schottky diode detector including a Schottky diode having a first terminal coupled to the antenna and having a second terminal; and

means for driving current through both the antenna and the Schottky diode in a direction from the second terminal to the first terminal.

133. A system comprising:

an antenna;

a transponder including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode; and

means for driving current through both the antenna and the Schottky diode in a direction from the anode to the cathode.

134. A radio frequency communications system comprising:

an antenna;

an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector;

a current source connected to the cathode to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

135. A radio frequency communications system comprising:

an antenna;

an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector; and

a current source connected to the anode to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

136. A system comprising:

an antenna;

a transponder including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode; and

means for driving current through both the antenna and the Schottky diode in a direction from the anode to the cathode.

137. A method for realizing an improved radio frequency detector for use in a radio frequency identification device (RFID), the method comprising the following steps:

providing an integrated circuit and an antenna, the integrated circuit having a receiver and a transmitter, the integrated circuit further having a Schottky diode and a current source, with the Schottky diode in operation being coupled to the antenna and the current source, the Schottky diode and antenna cooperating there between to form an inductorless radio frequency detector;

applying a supply of power to the integrated circuit device from a battery; and

applying a desired current across the Schottky diode to impart a desired impedance there across relative to the impedance of the antenna.

138. A frequency lock loop comprising:

a current controlled oscillator including a plurality of selectively engageable current mirrors, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the current mirrors including transistors operating in a subthreshold mode.

139. A frequency lock loop in accordance with claim 138 and further comprising a current source including a thermal voltage generator, and wherein the selected current mirrors multiply up the current from the current source to a current for controlling the frequency of oscillation.

140. A frequency lock loop in accordance with claim 138 wherein the current mirrors are arranged in selectable groups of varying numbers of transistors to define a binary weighting scheme.

141. A frequency lock loop in accordance with claim 140 and further comprising digital select lines, and wherein the groups are selected by signals on the digital select lines.

142. An integrated circuit comprising a receiver, a transmitter, and a frequency lock loop including a current source having a thermal voltage generator, a current controlled oscillator having a plurality of selectively engageable current mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the current mirrors including transistors operating in a subthreshold mode.

143. A frequency lock loop in accordance with claim 142 wherein the current mirrors are arranged in selectable groups of varying numbers of transistors to define a binary weighting scheme.

144. A frequency lock loop in accordance with claim 143 and further comprising digital select lines, and wherein the groups are selected by signals on the digital select lines.

145. A timing oscillator that consumes less than one milliAmp.

146. A method of constructing a frequency lock loop including a current controlled oscillator having a plurality of selectively engageable current mirrors, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising selecting current mirrors to vary frequency of operation, and operating transistors in the current mirrors in subthreshold mode.

147. A method in accordance with claim 146 and further comprising using a current source including a thermal voltage generator, and arranging the current mirrors so the engaged current mirrors multiply up the current from the current source to a current for controlling the frequency of oscillation.

148. A method in accordance with claim 146 and further comprising arranging the current mirrors in selectable groups of varying numbers of transistors to define a binary weighting scheme.

149. A method in accordance with claim 148 and further comprising selecting the groups using digital signals.

150. A method of operating an integrated circuit including a receiver, a transmitter, and a frequency lock loop including a current source having a thermal voltage generator, a current controlled oscillator having a plurality of selectively engageable current mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising engaging selected current mirrors and operating transistors in the current mirrors in a subthreshold mode.

151. A method in accordance with claim 150 and further comprising arranging the current mirrors in selectable groups of varying numbers of transistors to define a binary weighting scheme.

152. A method in accordance with claim 151 and further comprising selecting the groups using signals on digital select lines.

153. An amplifier powered by a selectively engageable voltage source, the amplifier comprising:

first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors;

a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output;

selectively engageable resistances between the voltage source and respective inputs of the differential amplifier and defining, with the coupling capacitors, the high pass characteristics of the circuit; and

second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values that the first mentioned resistances, the second resistances being engaged then disengaged in response to the voltage source being engaged.

154. An amplifier in accordance with claim 152 and further comprising coupling capacitors respectively connected to the first and second electrodes.

155. An amplifier in accordance with claim 152 and further comprising a voltage divider, and wherein the first mentioned and second resistances are connected to the voltage source via the voltage divider.

156. An amplifier in accordance with claim 152 wherein the first mentioned resistances comprise respective transistors.

157. An amplifier in accordance with claim 152 wherein the first mentioned resistances comprise respective p-type transistors.

158. An amplifier in accordance with claim 152 wherein the second resistances comprise respective transistors.

159. An amplifier in accordance with claim 152 wherein the second resistances comprise respective p-type transistors.

160. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a receiver receiving radio frequency commands from an interrogation device, and a transmitter transmitting a signal identifying the device to the interrogator, the integrated circuit switching between a sleep mode, and a microprocessor on mode, in which more power is consumed than in the sleep mode, if the microprocessor determines that a signal received by the receiver is a radio frequency command from an interrogation device, the integrated circuit further including an amplifier powered by a selectively engageable voltage source engaged in the microprocessor on mode but not in the sleep mode, the amplifier including first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors, a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output, selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values that the first mentioned resistances, the second resistances being engaged then disengaged in response to the integrated circuit switching from the sleep mode to the microprocessor on mode.

161. A radio frequency identification device in accordance with claim 160 and further comprising coupling capacitors respectively connected to the first and second electrodes.

162. A radio frequency identification device in accordance with claim 160 and further comprising a voltage divider, and wherein the first mentioned and second resistances are connected to the voltage source via the voltage divider.

163. A radio frequency identification device in accordance with claim 160 wherein the first mentioned resistances comprise respective transistors.

164. A radio frequency identification device in accordance with claim 160 wherein the first mentioned resistances comprise respective p-type transistors.

165. A radio frequency identification device in accordance with claim 160 wherein the second resistances comprise respective transistors.

166. A radio frequency identification device in accordance with claim 160 wherein the second resistances comprise respective p-type transistors.

167. A method of speeding power up of an amplifier stage powered by a voltage source and including first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors; a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; and selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the method comprising:

shorting around the selectively engageable resistances for a predetermined amount of time in response to the voltage source being engaged.

168. A method in accordance with claim 167 wherein the shorting step comprises engaging selectively engageable second resistances respectively connected in parallel with the first mentioned resistances and having respective resistance values lower than the first mentioned resistances.

169. A radio frequency communications system comprising:

an antenna;

an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector, the integrated circuit further including a clock recovery circuit recovering a clock from rising edges only of a signal at the output of the Schottky diode detector; and

a current source connected to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

170. A radio frequency communications system comprising:

an antenna;

an integrated circuit including a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector, the integrated circuit further including a clock recovery circuit recovering a clock from falling edges only of a signal at the output of the Schottky diode detector; and

a current source connected to drive current through the antenna and the Schottky diode in a direction from the anode to the cathode.

171. A method of recovering a clock in a radio frequency communications system, the method comprising:

providing an antenna;

providing a receiver having a Schottky diode detector including a Schottky diode having an anode coupled to the antenna and having a cathode, the Schottky diode detector further including a capacitor connected between the cathode and ground, and including a capacitor having a first contact connected to the cathode and having a second contact defining an output of the Schottky diode detector;

driving current through the antenna and the Schottky diode in a direction from the anode to the cathode; and

recovering a clock from rising edges only of a signal at the output of the Schottky diode detector.

172. A method of recovering a clock in a radio frequency communications system, the method comprising:

providing an antenna;

providing a receiver having a Schottky diode detector including a Schottky diode having a cathode coupled to the antenna and having an anode, the Schottky diode detector further including a capacitor connected between the anode and ground, and including a capacitor having a first contact connected to the anode and having a second contact defining an output of the Schottky diode detector;

driving current through the antenna and the Schottky diode in a direction from the anode to the cathode; and

recovering a clock from falling edges only of a signal at the output of the Schottky diode detector.

173. A stage for a voltage controlled oscillator, the stage comprising:

a first transistor having a control electrode defining a first input, and having first and second power electrodes, the first power electrode defining a first node;

a second transistor having a control electrode defining a second input, and having first and second power electrodes, the first power electrode of the second transistor defining a second node;

a current source connected to the second power electrodes of the first and second transistors and directing current away from the second power electrodes of the first and second transistors; and

means defining a variable resistance connecting the first and second nodes to a supply voltage.

174. A stage for a voltage controlled oscillator, the stage comprising:

a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain;

a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain;

a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source;

a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source;

a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the first and second n-channel transistors;

a first resistor connected between the supply voltage and the drain of the first n-type transistor;

a second resistor connected between the supply voltage and drain of the second n-type transistor;

a first source follower having an input connected to the first node and having an output defining a first output of the stage; and

a second source follower having an input connected to the second node and having an output defining a second output of the stage.

175. A transmitter including a ring oscillator having a chain of stages, each stage comprising:

a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain;

a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain;

a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source;

a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source;

a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the first and second n-channel transistors;

a first resistor connected between the supply voltage and the drain of the first n-type transistor;

a second resistor connected between the supply voltage and drain of the second n-type transistor;

a first source follower having an input connected to the first node and having an output defining a first output of the stage; and

a second source follower having an input connected to the second node and having an output defining a second output of the stage.

176. A method of varying frequency in a stage of a voltage controlled oscillator having two input transistors having gates defining input nodes and having drain to source paths adapted to be connected between a supply voltage and a current source, the method comprising providing an impedance between the input transistors and the supply voltage, and varying the impedance.

177. A frequency doubler comprising:

a first Gilbert cell;

a second Gilbert cell coupled to the first Gilbert cell;

a frequency generator configured to apply a first sinusoidal wave to the first Gilbert cell; and

a phase shifter applying a sinusoidal wave shifted from the first sinusoidal wave to the second Gilbert cell.

178. A frequency doubler comprising:

a first Gilbert cell including a first pair of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair having a gate defining a first input node and a first one of the transistors of the second pair having a gate connected to the first input node, a second one of the transistors of the first pair having a gate defining a second input node and a second one of the transistors of the second pair having a gate connected to the second input node, the first transistor of the first pair having a drain, and the second transistor of the second pair having a drain connected to the drain of the first transistor of the first pair, the second transistor of the first pair having a drain, and the first transistor of the second pair having a drain connected to the drain of the second transistor of the first pair, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair having a drain connected to the source of the second transistor of the first pair, the second transistor of the third pair having a drain connected to the source of the second transistor of the second pair, and a current source connected to the sources of the third pair and forward biasing the third pair, the second transistor of the third pair having a gate defining a third input node, and the first transistor of the third pair having a gate defining a fourth input node; and

a second Gilbert cell including a first pair of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair of the second cell having a gate defining a first input node and a first one of the transistors of the second pair of the second cell having a gate connected to the first input node of the second cell, a second one of the transistors of the first pair of the second cell having a gate defining a second input node of the second cell and a second one of the transistors of the second pair of the second cell having a gate connected to the second input node of the second cell, the first transistor of the first pair of the second cell having a drain, and the second transistor of the second pair of the second cell having a drain connected to the drain of the first transistor of the first pair of the second cell, the second transistor of the first pair of the second cell having a drain, and the first transistor of the second pair of the second cell having a drain connected to the drain of the second transistor of the first pair of the second cell, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair of the second cell having a drain connected to the source of the second transistor of the first pair of the second cell, the second transistor of the third pair of the second cell having a drain connected to the source of the second transistor of the second pair of the second cell, and a current source connected to the sources of the third pair of the second cell and forward biasing the third pair of the second cell,

the second transistor of the third pair of the second cell having a gate defining a third input node of the second cell, and the first transistor of the third pair of the second cell having a gate defining a fourth input node of the second cell; the drain of the second transistor of the first pair of the second cell being connected to the drain of the second transistor of the first pair of the first cell, the drain of the second transistor of the second pair of the second cell being connected to the drain of the second transistor of the second pair of the second cell, the first input node of the second cell being connected to the fourth input node of the first cell, the third input node of the second cell being connected to the second input node of the first cell, and the fourth input node of the second cell being connected to the first input node of the first cell.

179. A method of doubling frequency without using a feedback loop, the method comprising:

providing a first Gilbert cell;

providing a second Gilbert cell coupled to the first Gilbert cell;

applying a first sinusoidal wave to the first Gilbert cell; and

applying a sinusoidal wave shifted from the first sinusoidal wave to the second Gilbert cell.

180. A pseudo random number generator comprising:

a linear feedback shift register switchably operable in a first mode, and in a second mode wherein the shift register consumes more power than in the first mode.

181. A method of generating a pseudo random number, the method comprising:

providing a linear feedback shift register;

providing an oscillator which generates clock signals used by the linear feedback shift register for shifting; and

providing a first power level to the oscillator when a pseudo random number is required, and providing a second power level, lower than the first power level, to the oscillator at other times.

182. A method of generating a pseudo random number, the method comprising:

providing a linear feedback shift register;

providing an oscillator which generates clock signals used by the linear feeback shift register for shifting; and operating the oscillator at a first frequency in response to a request for a pseudo random number, and operating the oscillator at a second frequency lower than the first frequency after the pseudo random number is generated.

183. A method in accordance with claim 182 and further comprising supplying power to the oscillator from a thermal voltage generator to cause the oscillator to operate at the second frequency.

184. A system comprising:

a microprocessor operating at a frequency;

a linear feedback shift register operable in a low power mode, wherein the shift register operates at a frequency below the frequency of the microprocessor, and a high power mode wherein the shift register consumes more power than in the low power mode, operates at the frequency of the microprocessor, and shifts data into the microprocessor.

185. A radio frequency identification device comprising:

an integrated circuit including a receiver, a transmitter, a thermal voltage generator, a microprocessor operating at a frequency, a linear feedback shift register operable in a low power mode, wherein the shift register operates at a frequency below the frequency of the microprocessor, and a high power mode wherein the shift register consumes more power than in the low power mode, operates at the frequency of the microprocessor, and shifts data into the microprocessor, an oscillator supplying clock signals to the shift register, and current mirrors supplying current to each stage of the shift register, the current mirrors being referenced to the thermal voltage generator when the shift register is in the low power mode, and, when the shift register is in the high power mode, connected to a supply voltage potential greater than the potential provided by the thermal voltage generator.

186. A method of generating a pseudo random number, the method comprising:

providing a thermal voltage generator, a linear feedback shift register, an oscillator supplying clock signals to the shift register, and current mirrors supplying current to each stage of the shift register;

referencing the current mirrors to the thermal voltage generator when no pseudo random number is required; and

connecting the current mirrors to a supply voltage potential greater than the potential provided by the thermal voltage generator when a pseudo random number is required.

187. An integrated circuit comprising a receiver and a transmitter sharing a common antenna.

188. A method of using an integrated circuit including a receiver and a transmitter, the method comprising connecting the receiver and transmitter to a common antenna.

189. An integrated circuit comprising:

a die including a transmitter having an antenna output and a detector having an antenna input;

a package housing the die;

a first contact connected to the antenna output and accessible from outside the package;

a second contact connected to the antenna input and accessible from outside the package; and

a short electrically connecting the first contact to the second contact outside the package.

190. A method of using an integrated circuit including a die having a transmitter including an antenna output and a detector including an antenna output, the integrated circuit further including a package housing the die, a first contact connected to the antenna output and accessible from outside the package, and a second contact connected to the antenna input and accessible from outside the package, the method comprising:

electrically shorting the first contact to the second contact outside the package.

191. A transceiver comprising:

an antenna having a first end connected to a bias voltage, and having a second end;

a detector including a Schottky diode having an anode connected to the second end of the antenna; and

a transmitter having an output connected to the second end of the antenna.

192. A transceiver in accordance with claim 191 wherein the Schottky diode has a cathode, and further comprising a current source directing current in the direction from the anode to the cathode.

193. A transceiver in accordance with claim 191 wherein the receiver and transmitter do not operate simultaneously.

194. A transceiver in accordance with claim 191 wherein the Schottky diode has a cathode, and wherein the detector and transmitter do not operate simultaneously, the transceiver further comprising a current source directing current in the direction from the anode to the cathode, and a pullup transistor connected to the cathode and configured to connect the cathode to the bias voltage when the transmitter is operating.

195. A radio frequency identification device comprising:

an integrated circuit including both a receiver and a transmitter;

a first antenna connected to the receiver; and

a second antenna connected to the transmitter.

196. A radio frequency identification device in accordance with claim 195 wherein the receiver includes a Schottky diode having a cathode and an anode, and further comprising a current source directing current in the direction from the anode to the cathode.

197. A radio frequency identification device in accordance with claim 195 wherein the receiver and transmitter do not operate simultaneously.

198. A transceiver comprising:

a loop antenna having a first end connected to a bias voltage, and having a second end;

a second antenna;

a detector including a Schottky diode having an anode connected to the second end of the antenna; and

a transmitter having an output connected to the second antenna.

199. A transceiver in accordance with claim 198 wherein the Schottky diode has a cathode, and further comprising a current source directing current in the direction from the anode to the cathode.

200. A transceiver in accordance with claim 198 wherein the receiver and transmitter do not operate simultaneously.

201. A transceiver comprising:

an antenna having a first end connected to a bias voltage, and having a second end;

a detector including a Schottky diode having an anode connected to the second end of the antenna; and

an active transmitter having an output connected to the second end of the antenna.

202. A transceiver in accordance with claim 201 wherein the Schottky diode has a cathode, and further comprising a current source directing current in the direction from the anode to the cathode.

203. A transceiver in accordance with claim 201 wherein the receiver and transmitter do not operate simultaneously.

204. A transceiver in accordance with claim 201 wherein the Schottky diode has a cathode, and wherein the detector and transmitter do not operate simultaneously, the transceiver further comprising a current source directing current in the direction from the anode to the cathode, and a pullup transistor connected to the cathode and configured to connect the cathode to the bias voltage when the transmitter is operating.

205. A transceiver comprising:

an antenna having a first end, and having a second end;

a detector including a Schottky diode having a cathode connected to the second end of the antenna and defining a potential at the second end of the antenna, the first end of the antenna being connected to a potential lower than the potential of the second end of the antenna; and

a backscatter transmitter including a transistor having a first power electrode connected to the first end of the antenna, a second power electrode connected to the second end of the antenna, and a control electrode adapted to have a modulation signal applied thereto.

206. A transceiver in accordance with claim 205 and further comprising a current source directing current in the direction from the anode to the cathode.

207. A transceiver in accordance with claim 205 wherein the receiver and transmitter do not operate simultaneously.

208. A transceiver in accordance with claim 205 and further comprising an integrated circuit package housing the detector and transmitter, and wherein the antenna is external of the package.

209. A transceiver comprising:

a loop antenna having a first end connected to a bias voltage, and having a second end;

a detector including a Schottky diode having an anode connected to the second end of the antenna;

a backscatter transmitter having a first output and having a second output;

a capacitor connected between the first output and the first end of the antenna; and

a capacitor connected between the second output and the second end of the antenna.

210. A transceiver in accordance with claim 209 wherein the Schottky diode has a cathode, and further comprising a current source directing current in the direction from the anode to the cathode.

211. A transceiver in accordance with claim 209 wherein the receiver and transmitter do not operate simultaneously.

212. A transceiver in accordance with claim 209 and further comprising an integrated circuit package housing the detector and transmitter, and wherein the first and second capacitors are external of the package.

213. A method of configuring a transceiver including a backscatter transmitter having first and second outputs, and a detector having a Schottky diode including an anode, the method comprising:

applying a bias voltage to a first end of an antenna;

connecting a second end of the antenna to the anode;

connecting a capacitor between the first output and the first end of the antenna; and

connecting a capacitor between the second output and the second end of the antenna.

214. A method in accordance with claim 213 wherein the Schottky diode has a cathode, and further comprising directing current in the direction from the anode to the cathode.

215. A method in accordance with claim 213 wherein the receiver and transmitter do not operate simultaneously.

216. A method in accordance with claim 213 and further comprising housing the detector and transmitter in an integrated circuit package, and connecting the first and second capacitors external of the package.

217. A method of arranging a transceiver including a backscatter transmitter and a detector having a Schottky diode including a cathode, the method comprising:

connecting a first end of an antenna to a ground potential;

connecting a second end of the antenna to the cathode; and

connecting a first power electrode of a transistor to the first end of the antenna;

connecting a second power electrode connected to the second end of the antenna; and

connecting a control electrode of the transistor to a modulation signal.

218. A method in accordance with claim 217 and further comprising a current source directing current in the direction from the anode to the cathode.

219. A method in accordance with claim 217 wherein the receiver and transmitter do not operate simultaneously.

220. A method in accordance with claim 217 and further comprising housing the detector and transmitter in an integrated circuit package, and locating the antenna external of the package.

221. A method of determining when a phase lock loop achieves frequency lock relative to a desired frequency, the phase lock loop including a voltage controlled oscillator having a control node and oscillating at a frequency responsive to the voltage applied to the control node, the method comprising:

crossing the voltage that would result in the phase lock loop tracking the desired frequency in a first direction;

crossing the voltage that would result in the phase lock loop tracking the desired frequency in a second direction opposite the first direction; and

indicating that frequency lock has been achieved.

222. A method in accordance with claim 221 and further comprising adjusting the voltage in the first direction after the second mentioned crossing step and before the indicating step.

223. A method in accordance with claim 221 wherein the first mentioned crossing comprises adjusting, using steps, the voltage applied to the control node.

224. A method in accordance with claim 223 wherein the second mentioned crossing comprises adjusting the voltage applied to the control node using steps smaller than the steps used in the first mentioned crossing.

225. A method in accordance with claim 221 and further comprising adjusting the voltage in the first direction after the second mentioned crossing step and before the indicating step, and wherein the adjusting comprises using a step smaller than the steps used in the first mentioned crossing.

226. A method of determining when frequency lock occurs relative to a desired frequency, the method comprising:

providing a phase lock loop including a voltage controlled oscillator that oscillates at a frequency responsive to voltage applied to the voltage controlled oscillator;

applying a voltage to the voltage controlled oscillator to produce a frequency of oscillation less than the desired frequency;

increasing the voltage applied to the voltage controlled oscillator using one or more steps of a first size;

increasing the voltage applied to the voltage controlled oscillator using one or more steps of a second size smaller than the first size;

decreasing the voltage applied to the voltage controlled oscillator using one or more steps of a third size smaller than the second size;

increasing the voltage applied to the voltage controlled oscillator using a step of the third size; and

indicating that lock has occurred in response to the increase of the step of the third size.

227. A method in accordance with claim 226 wherein the phase lock loop tracks a timing signal.

228. A method in accordance with claim 226 wherein the voltage controlled oscillator has a control node, and wherein the voltage controlled oscillator oscillates at a frequency responsive to the voltage applied to the control node.

229. A method of determining when a phase lock loop achieves frequency lock relative to a desired frequency, the phase lock loop including a voltage controlled oscillator having a control node and oscillating at a frequency responsive to the voltage applied to the control node, the method comprising:

increasing the voltage applied to the control node to a voltage above the voltage that would result in the phase lock loop tracking the desired frequency;

decreasing the voltage applied to the control node to a voltage below the voltage that would result in the phase lock loop tracking the desired frequency; and

increasing the voltage applied to the control node and indicating that frequency lock has been achieved.

230. A method in accordance with claim 229 wherein the first mentioned increasing of the voltage applied to the control node comprises increasing in steps the voltage applied to the control node.

231. A method in accordance with claim 230 wherein the decreasing of the voltage applied to the control node comprises decreasing the voltage applied to the control node using steps smaller than the steps used in the first mentioned increasing of the voltage applied to the control node.

232. A method in accordance with claim 230 wherein the second mentioned increasing of the voltage applied to the control node comprises increasing the voltage applied to the control node using a step smaller than the steps used in the first mentioned increasing of the voltage applied to the control node.

233. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit periodically switching between a sleep mode, and a receiver-on mode in which more power is consumed than in the sleep mode, and further including a selectively engageable timer preventing switching from the sleep mode to the receiver-on mode for a predetermined amount of time.

234. A radio frequency identification device in accordance with claim 233 wherein the timer is a countdown timer.

235. A radio frequency identification device in accordance with claim 233 wherein the timer comprises a counter.

236. A radio frequency identification device in accordance with claim 233 wherein the timer is set by a radio frequency signal received by the receiver.

237. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit periodically switching between a sleep mode, and a receiver-on mode in which more power is consumed than in the sleep mode, and further including means for selectively preventing switching from the sleep mode to the receiver-on mode for a predetermined amount of time.

238. A radio frequency identification device in accordance with claim 237 wherein the means comprises a countdown timer.

239. A radio frequency identification device in accordance with claim 237 wherein the means comprises a counter.

240. A radio frequency identification device in accordance with claim 237 wherein the means prevents switching from the sleep mode in response to a radio frequency signal received by the receiver.

241. A radio frequency identification device comprising:

an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit being switchable between a sleep mode, and a mode in which more power is consumed than in the sleep mode, the integrated circuit being switched from the sleep mode to the mode in which more power is consumed in response to a direct sequence spread spectrum modulated radio frequency signal being received by the receiver which has a predetermined number of transitions within a certain period of time, the integrated circuit further including a selectively engageable timer which prevents switching from the sleep mode for a period of time regardless of whether a signal is subsequently received by the receiver which has the predetermined number of transitions within a certain period of time.

242. A radio frequency identification device in accordance with claim 241 wherein the timer is a countdown timer.

243. A radio frequency identification device in accordance with claim 241 wherein the timer comprises a counter.

244. A radio frequency identification device in accordance with claim 241 wherein the timer is set by a radio frequency signal received by the receiver.

245. A method for conserving power in a radio frequency identification device, the method comprising:

periodically switching from a sleep mode to a receiver on mode and performing tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present; and

selectively disabling the periodic switching from the sleep mode for a predetermined amount of time.

246. A method for conserving power in accordance with claim 245 wherein the selective disabling is performed in response to a radio frequency command.

247. A method for conserving power in accordance with claim 245 wherein the selective disabling is performed in response to a radio frequency command, and wherein the selective disabling cannot be cancelled by a subsequent radio frequency command.

248. A method in accordance with claim 245 wherein the step of selectively disabling comprises setting a timer.

249. A method in accordance with claim 245 wherein the step of selectively disabling comprises setting a countdown timer.

250. A method in accordance with claim 245 wherein the predetermined amount of time is selected via a radio frequency command.

251. A method in accordance with claim 245 wherein the predetermined amount of time is variable.

252. A method in accordance with claim 245 wherein the predetermined amount of time is selectable from a number of available amounts of time.